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THE AMX FLY-BY-WIRE SYSTEM

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1. INTRODUCTION

The AMX aircraft is a single engine fighter primarily for the Italian and Brazilian Air Forces. The aircraft is designed specifically for ground attack and the Flight Control System (FCS) provides full authority three axis fly-by-wire control to give Class 1 handling characteristics for its operational flight envelope.

The FCS provides autostabilization and autopilot facilities, and operates in conjunction with the stabilizer, spoiler and rudder actuators to give a safety critical failure rate of not more than 1×10^{-7} per flight hour. In the event of loss of the FCS, limited reversionary control is provided by the elevators and ailerons with emergency electric pitch trim on the stabilizer.

Pitch axis control is achieved by movement of the stabilizer, yaw control by movement of the rudder, and roll control by differential movement of the left and right spoilers. There are no asymmetric left and right stabilizer surface movements.

Damping of aircraft motion about the pitch, roll and yaw axes is provided by control surface commands computed from the outputs of the three axis rate gyro unit.

Stabilizer and rudder trim position changes may be demanded by the pilot by operation of cockpit switches. The trim position is stored electronically.

An airbrake facility is implemented by commanding simultaneous extension of both left and right spoilers whilst retaining full differential operation for roll control.

The lift dump facility may be selected by the pilot prior to touch down and is implemented in a similar manner to airbrake except that interlock devices ensure that the throttle lever has been moved to the IDLE position and the aircraft weight has been put on at least one wheel. Again full differential operation of the spoiler is retained.

The control signals developed within the EFCS are scheduled with airdata signals. These signals are derived from duplex airdata units which are part of the EFCS.

The logic sub-system allows engagement and reset of the above facilities prior to take off or in flight. A Training Mode is available in the logic which allows for disconnection and re-connection of the fly by wire control facilities.

The FCS consists of two identical self monitored Flight Control Computers (FCCs), each driving one lane of the stabilizer and rudder actuators and one pair of spoiler actuators. The stabilizer and rudder actuators are designed with duplex force summing first stages, and the spoilers are arranged in two pairs - inboard and outboard.

The control surface position commands are computed from signals proportional to the displacement of the control stick and rudder pedal controls. The displacements of the aircraft controls are measured by quadruplex electrical potentiometer pick-offs.

The customer specifically required that the stick and rudder pedal primary command functions be implemented in analogue computing technology to ease the certification difficulties of a digital system. However the low bandwidth limited authority functions, such as the trim and airdata schedules, could be computed using either analogue or digital processing technology. In addition the customer required that full provision be included for an autopilot with inputs provided via a MIL-STD-1553B data link.

2. OUTLINE DESCRIPTION

The design of the aircraft has placed considerable emphasis on survivability and this has been reflected in the arrangement of the FCS. In order to achieve a high level of mission reliability in addition to any single failure of the FCS, the following failure combinations may occur without any degradation of the mission plan.

Either EFCS lane and the Rate Gyro Unit
Both Airdata Units and one EFCS lane
Hydraulic Lane A and EFCS Lane 1
Hydraulic Lane B and EFCS Lane 2
Either electrical supply and one EFCS lane

It is intended that the aircraft abort the mission and return to base after the following failure combinations:-

EFCS Lane 1 and Hydraulics Lane B
EFCS Lane 2 and Hydraulics Lane A
Both EFCS lanes
Both electrical supplies
Reversionary Control System and one EFCS Lane

The general arrangement for the Electronic Flight Control System is shown in Figure 2.1. Two Flight Control Computers (FCCs) are arranged as a duplex self monitored system to give first failure operation and to meet the overall integrity requirements for the system.

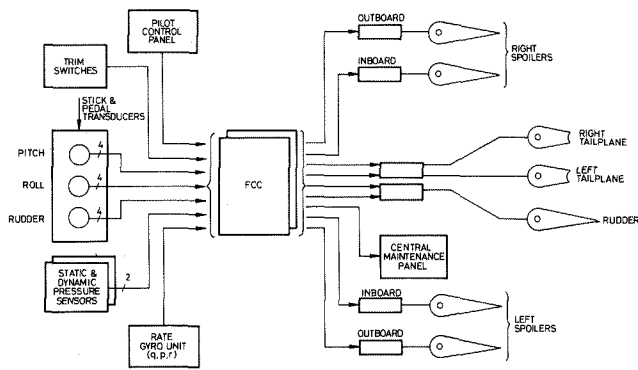


Figure 2.1 EFCS General Arrangement

FCC₁ drives one lane of the stabilizer and rudder actuators, and the inboard pair of spoiler actuators. FCC₂ drives the second lane of the stabilizer and rudder actuators, and the outboard pair of spoilers actuators. Both stabilizer and rudder drives are forced summed to provide a common output to their respective control surfaces.

In the event of a failure of one computer or a lane of the electric supplies or hydraulics, the lane is isolated and the system remains fully operational using the healthy computer, electric supply and hydraulics.

Quadruplex stick and pedal transducer signals are input to the command and the monitor lanes of each FCC. The static and dynamic pressures are provided by duplex airdata units. The 3 axis rate gyros, having limited authority, are simplex. Trim demands and other pilot's control panel signals are fed to both command and monitor channels of each FCC.

The dc electrical supplies to the EFCS consist of duplicated ac generators and transformer rectifier units (TRU), arranged so that both FCCs remain fully operative after single failures of either the generators or the TRUs. The bus bars are not battery supported.

The actuators operate from duplicated hydraulic supplies with Hydraulic System A supplying FCS Lane 1 and Hydraulic System B supplying FCS Lane 2. The hydraulic systems are not cross connected.

The spoiler actuators are single hydraulic rams operating from one hydraulic supply, with each ram being controlled by a single servo valve. Redundant spoiler control is made available by duplication of the spoiler surfaces on both the right and left sides of the aircraft. A separate spoiler actuator is associated with each of these four surfaces. The effects of these actuators are summed aerodynamically.

The rudder actuator is a two stage actuator which consists of a pair of hydraulic rams mechanically coupled together to provide a common output to the rudder surface. Each of these rams is controlled by an independent servo valve.

The stabilizer actuator is also a two stage actuator which contains two rotary hydraulic motors coupled to a common output shaft arranged to give symmetrical motion of the two tailplane surfaces. The hydraulic pressure supplied to each motor is controlled via an independent servo valve.

The actuators have no hydro-mechanical failure logic or fail safe characteristics. However electro-mechanical solenoid valves are provided, so that either duplicated lane of actuation can be depressurized independently, allowing normal operation with only one lane operational. The flight control computers provide the actuator monitoring and logic to disconnect failed lanes.

3. EFCS ARCHITECTURE

3.1 Computer Architecture

A simplified schematic of the architecture is shown in Figure 3.1.

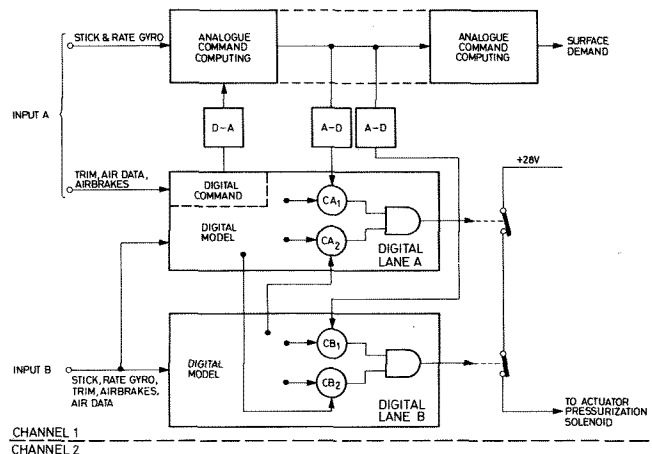


Figure 3.1 Computer Architecture

Precision analogue computing is used for the servo loops and to compute the primary command functions in order to minimize the differential between channel 1 and channel 2. Functions with a low bandwidth requirement are computed digitally. These include the gain scheduled functions of dynamic and static pressure, pitch and yaw trim, and control and engagement logic.

Particular attention has been given to the configuration of the sensor input signals of the digital lanes. The configuration shown gives the highest integrity, as the sensors have a failure rate which is significantly smaller than that of the computing lanes.

The two digital lanes (A and B) are arranged to perform different roles. Digital Lane A has a dual role, it generates the digitally implemented control functions and it acts as a monitor to the analogue command computing. Digital Lane B computes a complete model of the analogue and digitally implemented functions, and acts as a monitor to both the analogue command channel and Digital Lane A.

The monitoring is arranged such that each digital lane acts as an independent monitor of the analogue command computing. The mechanism by which this is achieved is shown diagrammatically in Figure 3.2, and it can be seen that the two processors are arranged on either side of the command computing each connected by its own A-D interface. Then outputs from the lane isolation logic in each digital lane are logically ANDed so that both digital lanes are required to set a healthy condition to energize the channel pressurization solenoids for each actuator. Signal differentials which exceed pre-determined thresholds, identified by either digital lane, cause disconnection of the failed channel.

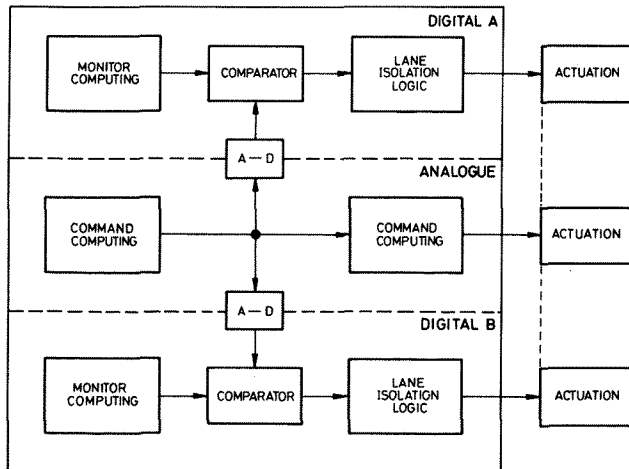


Figure 3.2 FCC Comparator Arrangement

Similarly the air data gain schedule and other functions computed in the two digital lanes, are crossfed and a failure condition identified by either digital lane disconnects the channel.

The processors are not synchronized in any way and therefore each processor requires one frame to sample the command computing and make a valid comparison. However, to minimize the risk of nuisance disconnections, a lane is isolated only after several consecutive data sample and computation cycles compute a failed condition. Nevertheless the computation cycle used by the system enables a lane isolation command to be initiated 50 milliseconds after a failure has occurred.

In addition to the command computing comparison monitors, comparison monitors are also incorporated to test the actual responses of certain system components against the expected responses. The components monitored in this way are the actuator position LVDT sensors and the servo valve monitors associated with each actuator input.

To provide adequate monitoring of the spool valve an analogue monitor is used. This compares the servo valve spool position with the servo valve demand current. Significant discrepancies cause the monitor to indicate a failed condition, and the appropriate actuator pressurization solenoid is de-energized after a time delay also optimized to minimize nuisance disconnections.

In order to minimize the surface movement once a failure has been registered in the computing, a switch sets the servo demand current to zero. As the actuator is active during depressurization, this has the effect of reducing the actuator rate while the actuator is being depressurized, thereby reducing the amplitude of the failure transient.

The architecture and monitoring have been configured to enable the EFCS to operate safely and minimize failure disconnect transients. This has been achieved with minimum hardware by making full use of digital computing techniques.

3.2 Force Sum Actuator Considerations

Force sum actuators are used for the rudder and stabilizer so that any surface movements which result from computing lane failures are minimized, not only by the performance of the computer monitoring system, but also by the creation of a force fight between the failed and healthy lanes. This is created in the following way.

The output of the rudder and stabilizer actuators are force summed. The servo valve demands cause changes in hydraulic fluid pressure which changes the actuators output force. Servo valve demands in the same sense give normal surface control. However opposing demands result in a force fight and the output will no longer respond to input commands. Therefore actuator main ram movements are either zero or very small.

This is an extremely effective method with the result that potentially large uncommanded surface movements are converted into zero or small surface displacements, allowing safe handling of the aircraft to be maintained.

In order that the actuators achieve their specified performance, the force sum servo valve command signals are required to be tightly matched over the full range of environmental conditions. If the command signals are not matched, then an effective deadspace is introduced into each surface control function chain, the amplitude of which, is directly proportional to the differential between the command signals.

However, the configuration suffers from the disadvantage, that in order to achieve the bandwidths and linearity required for normal operational performance, the maximum command computing lane signal differentials, are required to be considerably less than the tolerances of available sensors. In addition, the differentials are significantly increased by the normal tolerance build up of the electronic analogue computing hardware in each command channel.

The method chosen to equalize the two command signals, is to crossfeed and compare the spool valve demand signals in each command channel and compute a limited authority offset signal. When added to the demand signal the offset is sufficient to minimize the force sum differential on the outputs of the first stage of the actuator.

The limitation of this method is that the crossfeed signals provide positive feed forward signals to the servo command signals up to the maximum level determined by the authority limits.

Therefore a failure upstream of the equalization network automatically introduces a transient surface movement.

Since the authority limits must provide equalization between FCCs for both sensor and computing tolerances over the full range of environmental conditions, steps must be taken to minimize the error build up, so that the authority limits can be set to acceptable values. This is done by containing the tolerance build up to acceptable levels and by the introduction of consolidation points.

In order to evaluate the performance of the architecture and the monitoring system for the actuators and their associated servo loops, a comprehensive model of the configuration was simulated on a digital computer. This simulation was then used to determine the effectiveness of the monitoring system for a variety of normal operational and failure conditions.

4. FCC DESCRIPTION

4.1 Functional Configuration

Each Flight Control Computer (FCC) consists of an analogue command lane and two similar digital processing lanes as shown in Figure 4.1. The functions are split on a module by module basis.

Pitch computing modules take inputs from the pitch stick and pitch rate gyro and provide the demands to the stabilizer surface. Commands from the roll stick and roll rate gyro are processed on roll computing modules to control and position the inboard and outboard spoilers. Yaw computing modules control the rudder position in response to commands from the yaw pedal and yaw rate gyro.

These analogue modules receive analogue commands from Digital Lane A, which provides trim, airbrake and airdata scheduled gain functions for the respective axes via sample hold circuits. Disconnection switching for FCC disconnection/reset is provided by both Digital Lane A and Lane B.

The two digital processing lanes perform essentially the same functions. Digital Lane A however, forms part of the command lane as well as performing a monitor function, whereas Lane B provides an independent monitor function.

Analogue inputs from the aircraft sensors are buffered and filtered on the DC Analogue Input modules before being multiplexed and converted into digital data via the A/D Converter. This digital word is placed on the system bus and then into memory for processing. Similarly discrete signals are input to the processors under program control, via the system bus.

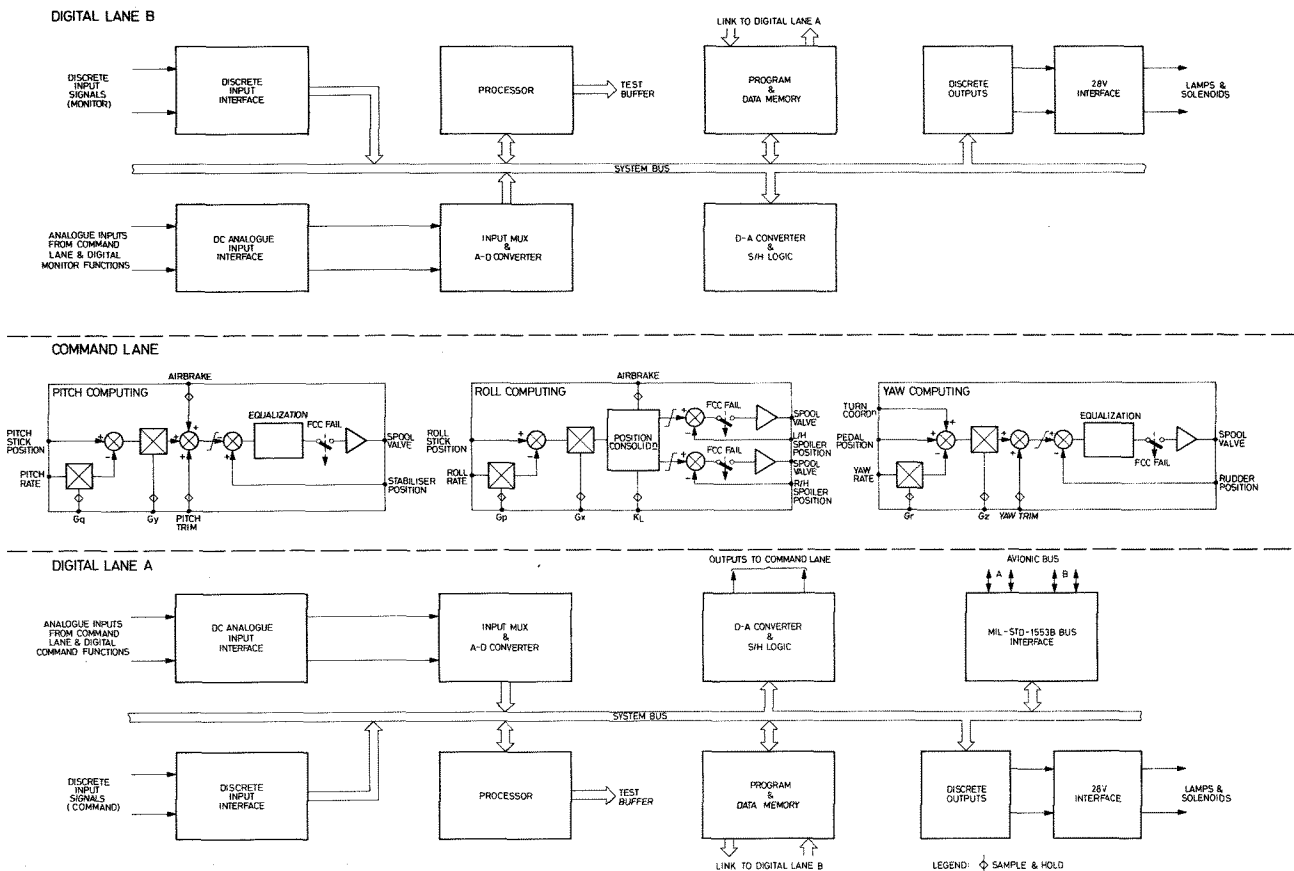


Figure 4.1 FCC Functional Configuration

4.2. Mechanical Design

Most modules in digital lanes A and B interface with their respective system bus, allowing information to pass between the various modules for processing.

The main program memory contains the instructions which enable all system functions to be carried out. The random access memory is used for temporary storage of information (including updating of inputs and outputs). The design also allows information to be cross fed between digital lanes A and B.

A 16 bit microprocessor, the Z8002, forms the heart of the Processor module. This micro, via a bi-directional buffer, interfaces with the system bus, and executes, in the correct sequence, instructions from the program/data store. A bi-directional test buffer is also incorporated onto the module and can be used in conjunction with a test set allowing external control of the memory and microprocessor.

The Power Supply Unit is a switched mode dc to dc converter operating from the 28V aircraft supply and it has been designed to absorb transient input voltage variations in excess of the requirements of MIL-STD-704D.

Full provision is included for two MIL-STD-1553B interface modules connected to the dual avionic bus. They will be used to provide the navigational, height and attitude information for the autopilot functions.

The Flight Control Computer is comprised of two separate items, the module Chassis, and the Power Supply Unit. Each item is manufactured as a one piece aluminium alloy investment casting and when combined together, form an extended 3/4 short ARINC 404A box. A general view of the FCC is shown in Figure 4.2.

The computer thermal management employed is the forced air / cold wall technique with bottom air entry (as per ARINC 404A) and front panel exhaust. When assembled the adjacent walls of the Power Supply and the Chassis form either side of the cooling air duct, thereby eliminating the need for a separate duct. The design makes efficient use of the available air and provides a very easy method of cleaning the duct.

Electrical interface with the aircraft is via two rear mounted, triple gang DPX connectors, and retention in the mounting tray utilizes these connectors at the rear and NAS 622 style hold down hooks at the front.

The modules are mounted vertically in guides that are an integral part of the chassis and plug into a horizontally mounted multilayer motherboard situated in the base of the computer.

The PCB modules consist of multilayer printed circuit boards incorporating integral thermal ladders, to which all active components are bonded, thereby conducting heat from the components to the computer walls.

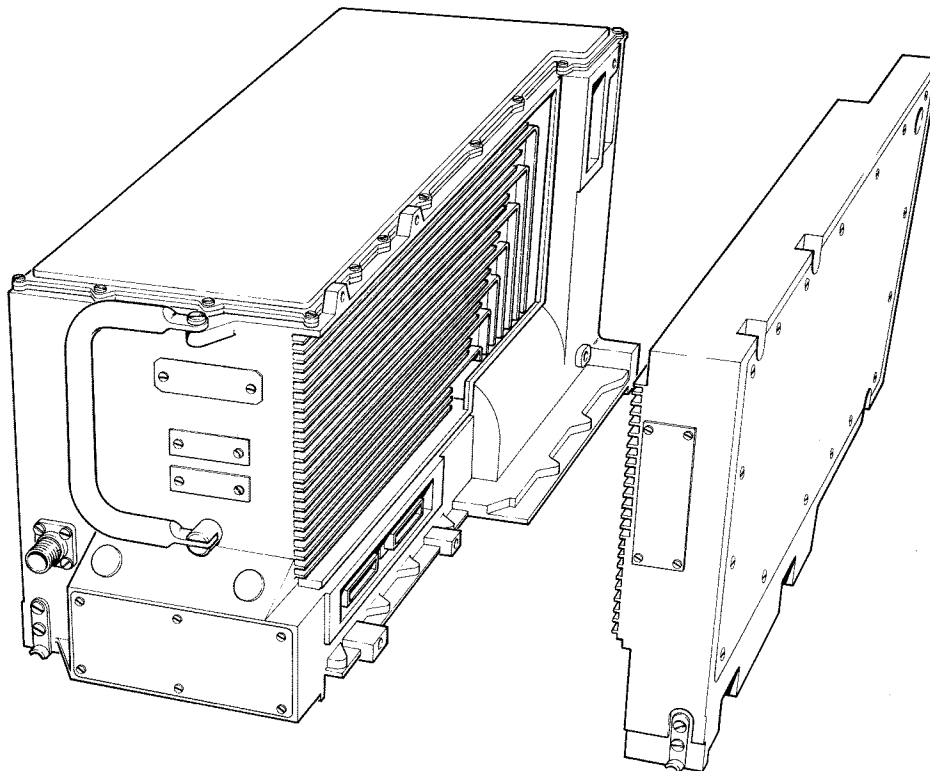


Figure 4.2 The Flight Control Computer

Efficient thermal transfer to the cold wall is achieved by use of a proprietary thermal clamp which enables insertion and extraction of the module with a small friction force between the module and the guides but provides a consistently high thermal contact pressure between the thermal ladder and guides, when the clamps are locked.

Module access is obtained by removal of a single EMI sealed top cover and access to the motherboard by removal of a similarly sealed bottom cover.

The total motherboard assembly, which includes all internal cables plus both the PSU and aircraft interfacing connectors, is removable as a single item by removing the bottom cover and the rear connector mounting plate.

Electrical segregation between DIGITAL Lane A, COMMAND, and DIGITAL Lane B is achieved in the following manner.

- At module level by cast-in segregation barriers in the computer chassis.
- Within the motherboard by separation of each of the three lanes by track free no-go areas between each lane.
- At the aircraft/computer interface connectors by utilization of the two physically separate connectors and by further segmentation within each connector.
- For the cableforms by provision of separate screened cable runs down either side of the computer.

In addition, the 28V electrical connections associated with the output circuits for the switches, solenoids and lamps have been collected and buffered onto two segregated 28V Interface modules to ensure that all the main computing electronics are fully isolated from the aircraft supplies.

4.3 Flight Resident Software

The Flight Resident Software is designed in accordance with the guidelines and procedures developed for high integrity fly-by-wire projects.

The essential requirement is visibility, and this is achieved by the use of simple software structures, clear requirements definition, thorough testing and design audit, detailed documentation, and rigorous production and configuration control.

Real time control is achieved by a hardware master interrupt timer which calls a non-interruptible Executive. The Executive then calls a number of frames in a defined sequence designed to give the required iteration rates for the various parameters.

To provide an indication of the scope of the program required for the AM-X FCS, a breakdown of the memory required for each major function is shown in Table 4.1.

Function	Memory Allocation (%)
Executive, Frame Control and On-Line Monitor	3
Initialization	2
Fly-By-Wire Control and Failure Logic	24
Autopilot (Provisional)	32
Pre-Flight BITE	39

Table 4.1 Flight resident software memory requirements

A unique function of the software is the choice of instruction set. Although the Z8002 microprocessor has a comprehensive instruction set, not all the instructions are compatible with the guidelines established for the development of high integrity software. For example, indirectly addressed instructions are prohibited.

In order not to make a substantial reduction in the throughput capacity of the microprocessor, the instruction set has been evaluated in terms of utility and auditability, and a subset list of preferred instructions has been identified.

The FRS has been structured from the functional relationships implied by the various computing tasks of the control laws and the FCC architecture into the following major segments:-

- Z8002 Computing
- On-Line Executive
- Links
- General routines (Sub-routines)
- In-Flight Monitoring
- Rudder
- Stabilizer
- Spoilers
- Airdata
- Logic
- Autopilot (Provisional)
- Pre-flight Checks

The structure is then further segmented into frames based on the iteration rate requirements of each function. This is shown in Figure 4.3.

For the in flight functions 4 frames are used to give the required iteration rates and the link structure controls the iteration rate of each function. In general the control laws and analogue monitoring functions are computed in each frame and the airdata and trim functions are computed once per program cycle.

During the normal operation of the FCC the two processor lanes are not synchronized in any way, and the various control and monitoring algorithms have been designed to take into account any timing differences that may occur. This has been done in order to ensure the independence of each digital lane.

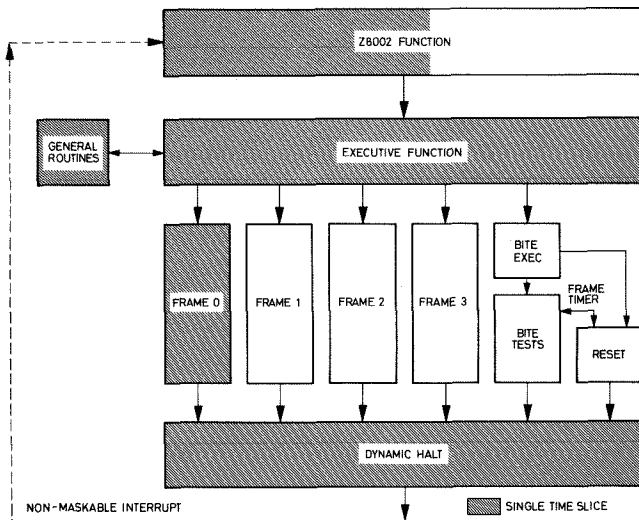


Figure 4.3 Program Segments

To provide confidence that the FCS is operating correctly, Pre-Flight BITE circuitry and software, have been incorporated to ensure that:-

- The various analogue system components including monitors, external sensors and actuators are operating correctly
- The computing functions are operating and interfacing correctly with all the required inputs and outputs.
- All inter-FCC connections are intact.

The versatility of the microprocessor enables comprehensive BITE testing to be implemented.

When the appropriate requests and interlocks are set for the Pre-Flight checks to be called, the Executive passes control to the PFC BITE Executive.

The Pre-Flight Checks are sub-divided into 3 main groups:-

- Automatic Tests
- Pilot Participation Tests
- Hydraulic System Dependent Tests

The automatic tests comprise a series of tests for the FCC hardware covering the processor and memories, the analogue computing and engagement logic.

The pilot participation tests cover the pilots controls, switches, lamps and the Reset function.

The hydraulic system dependent tests are those concerned with the actuators. These are principally designed to test the operability of each lane of the duplex actuators.

A special feature of the PFC BITE Executive allows the tests being carried out by each FCC to be co-ordinated.

5. COMPETITIVE FEATURES

5.1 Introduction

This Flight Control System contains a variety of features which make significant advances over existing systems. Many of the features are the result of the evolutionary development of technology, and combined, they provide a better product in terms of performance capability, ease of airworthiness certification, product design and life cycle costs. The main competitive features are described in the following sections.

5.2 Performance and Capability

The primary feature in terms of capability is that the system is a high availability full authority fly-by-wire system with no reversionary control being provided using the controlled surfaces. The system provides all the control necessary for high performance combat manoeuvrability, while the ailerons, elevators and electric pitch trim are only sufficient to maintain a basic level of 'return to base' handling qualities.

It also has full provision for a multi-mode autopilot including control stick steering designed to reduce pilot work load during the flight to and from the target area with the attitude, heading, altitude and other navigational data being fed to the FCC via dual MIL 1553 B data buses.

5.3 Airworthiness Certification

Since the techniques for certifying digital systems for use in high integrity applications are still being developed, considerable attention has been given to ensuring that no significant problems will arise in obtaining full airworthiness certification from the various authorities involved.

The primary feature of the system, from a certification viewpoint, is that the main command computing and servo loop functions are implemented in analogue technology which allows a conventional Failure Modes, Effects and Probability Analysis to be presented.

The digital processors, memories and interfaces are fully physically segregated and, although they have a common program, the program sequences are different and asynchronous. In the hypothetical event of a software defect not being detected by the monitors, the effect would be that an incorrect gain or bias would be set in the analogue command computing. It is then expected that the pilot would take appropriate overriding action depending on the severity of the effect and the prevailing redundancy of the equipment. Therefore even if the integrity assessment of the software is conceptually difficult for the certification authorities to accept, the design ensures that the risk of a safety critical condition, as a result of a common mode design defect in the software, is unlikely to be significant.

5.4 Microprocessor Implemented Functions

Full advantage has been taken of microprocessor technology to provide relatively large computing power in a small area. In addition high density EPROMs, Programmable Array Logic and other VLSI devices have been used.

The memory is large enough to provide a 3 axes fly-by-wire model and monitor function as well as the autopilot facility.

In order to appreciate the significance of the reduction in size achieved by the use of the microprocessor a comparison has been made of an equivalent analogue implementation. This estimate shows that an additional 40% of module area would be required, excluding any additional consolidation and monitoring necessary to provide adequate failure transient performance.

5.5 Cold-Wall Box Construction

This type of construction allows the use of contaminated air to remove the heat dissipated within the FCC without exposing the components directly to the cooling air. The thermal design ensures that the thermal gradient between the components and the cold wall are small, thereby virtually eliminating 'hot spots' and improving reliability. In addition, the computers operate for more than thirty minutes without any reduction in performance in the event that the supply of cooling air fails.

5.6 High Integrity Software

The procedures and methods, developed over a number of years for the design of safe software for fly-by-wire systems (eg Tornado, Jaguar FBW), have been incorporated in the Flight Resident Software for the AM-X project.

5.7 Life Cycle Cost

One of the main factors which influences the life cycle cost of a unit is its maintainability. Therefore when failure occurs, efficient diagnosis, easy access to the faulty device and a quick turn round time are required. The AM-X Flight Control System has been designed with this view in mind, the main features being:-

- Comprehensive Pre-Flight BITE allowing on-condition maintenance with the failure status being displayed on the Central Maintenance Panel. In addition a comprehensive test result data table may be accessed for off-aircraft evaluation of failures.
- Easy replacement of parts as follows:
 - All modules are plug in for easy access and replacement and require no in-situ adjustments.

The bolt on replaceable Power Supply Unit has been designed as a shallow depth box to provide easy access for test and component replacement.

The motherboard wiring harnesses connectors and back plate are an integral unit which is easily removable to facilitate repair.

• Support Equipment

The hardware has been specifically designed to be tested by an automatic test facility. A host ATE machine has been designated to test the EFCS and considerable use has been made of it during the development phase of the project to meet the programme delivery timescales and to ensure the effectiveness of the test programmes. It is envisaged that similar facilities will be used for second and third line maintenance.

6. CONCLUSION

A system has been designed to provide a comprehensive high performance fly-by-wire facility for an aircraft with an independent reversionary capability within strict weight and cost constraints.

The FCS was extensively tested on the flight control system rig and it successfully flew the first prototype aircraft on every flight throughout its flight envelope without any defect being noted.

Therefore the practicality of the design has been confirmed and the development programme can proceed with the addition of the autopilot and any other features that are required in complete confidence.

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R. B. Smith is employed by the Combat Aircraft Controls Division of GEC Avionics Limited, Rochester, England and Dott B. Tamagnone is employed by Aeritalia Gruppo Sistemi Avionici Ed Equipaggiamenti, Turin, Italy.